COMPONENT MINIMIZED MULTILEVEL INVERTER ARCHITECTURE FOR EFFICIENT STANDALONE SOLAR POWER CONVERSION

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Abstract

This paper introduces a high-resolution 31-level multilevel inverter (MLI) configuration characterized by a significantly reduced semiconductor switch count, specifically optimized for standalone solar photovoltaic (PV) applications. Traditional MLI architectures typically encounter trade-offs between the number of output levels and the complexity of the hardware; however, the proposed design utilizes only 13 power switches to achieve 31 levels. This is accomplished through a strategic binary-weighted asymmetric DC source management strategy, employing a voltage ratio of 1:2:4:8. To address the intermittent nature of solar irradiance, the system integrates a battery energy storage system (BESS) via bidirectional DC-DC converters, ensuring the stability of the DC-link capacitors and a continuous power supply. The performance of the system was validated through extensive MATLAB/Simulink simulations using a 2.5 kW induction motor load. The results demonstrate a voltage Total Harmonic Distortion (THD) of 2.86% and a current THD of 0.11%, which are well within the limits defined by international power quality standards. The proposed topology offers an efficient, low-cost, and high-fidelity power conversion solution for grid-isolated renewable energy systems, eliminating the requirement for bulky output filters and reducing electromagnetic interference.

Keywords *Multilevel Inverter (MLI), Total Harmonic Distortion (THD), Binary-weighted sources, Solar Photovoltaic, Battery Energy Storage, Bidirectional Converter*.

I. Introduction

The escalating global energy demand, coupled with the environmental concerns surrounding fossil fuel consumption, has positioned solar photovoltaic (PV) technology as a cornerstone of the modern renewable energy landscape [1]. Standalone solar energy conversion systems are particularly vital for delivering sustainable power to decentralized and grid-isolated regions, where they support essential activities such as continuous irrigation, rural farming, and water treatment processes [1], [3]. However, the integration of solar PV with AC loads necessitates sophisticated power electronic interfaces capable of maintaining high power quality despite the intermittent nature of solar irradiance. Traditional two-level inverters, while simple in design, generate significant harmonic distortion and subject motor loads to high dv/dt stress, leading to electromagnetic interference and reduced machine longevity. Multilevel inverters (MLIs) have emerged as a superior alternative by synthesizing a staircase output voltage that closely approximates a pure sine wave, thereby improving waveform quality and reducing harmonic

content [3]. Despite these advantages, classical MLI topologies—such as the Neutral Point Clamped (NPC) and Flying Capacitor (FC) inverters require an extensive number of power switches, clamping diodes, or balancing capacitors as the number of output levels increases [2], [4]. This increased component count leads to higher manufacturing costs, larger physical footprints, and increased power losses [7]. Recent advancements in power electronics have focused on developing topologies with a reduced device count to enhance cost-effectiveness and reliability [2], [6]. Asymmetric source management has been identified as an effective method to increase the number of output levels without a proportional increase in the number of semiconductor switches [5], [8]. While prior research successfully implemented 17-level outputs using simplified architectures [3], there remains a critical need for higher resolution to further minimize Total Harmonic Distortion (THD) and eliminate the need for bulky passive filters. This paper addresses these challenges by proposing a 13-switch, 31-level inverter topology utilizing a binary-weighted source configuration (1:2:4:8 ratio). By integrating a battery energy storage system (BESS) and bidirectional DC-DC converters, the proposed system ensures stable DC-link voltages and high-quality power delivery to a 2.5 kW induction motor, regardless of environmental fluctuations. This approach optimizes the level-to-switch ratio, satisfying international power quality standards while maintaining a streamlined hardware architecture.

II. Literature Review / Related Work

The evolution of multilevel inverter (MLI) technology is driven by the necessity to deliver high-quality power with minimal harmonic interference, particularly in standalone renewable energy frameworks. Recent literature has extensively explored various topological improvements to overcome the limitations of conventional systems.

The integration of solar photovoltaic (PV) systems for off-grid applications has been a primary focus, where researchers emphasize the importance of reliable power electronic interfaces for driving induction motors in remote areas [1]. In such standalone environments, the quality of the AC output is paramount to prevent motor overheating and vibration. Standard MLI topologies, such as the Neutral Point Clamped (NPC) and Cascaded H-Bridge (CHB), have been historically utilized to improve waveform quality; however, they require a significant number of semiconductor switches and auxiliary components, which increases the probability of component failure and overall system cost [2]. To mitigate the issues of high component count, recent studies have introduced "Reduced Device Count" (RDC) topologies. Mukundan et al. [3] proposed a novel MLI configuration that generates multiple voltage levels using only ten switches and two isolated DC sources. This research demonstrated that by employing asymmetric source management, higher resolution can be achieved without altering the basic circuit framework. Similarly, the work in [6] and [7] explored new MLI architectures that prioritize a reduction in the total blocking voltage (TBV) and the number of gate driver circuits, which are critical factors in enhancing the inverter's power density and economic viability. The strategy of utilizing asymmetric or binary-weighted DC sources has proven to be a game-changer in level synthesis. For instance, Lee et al. [5] implemented a 31-level inverter with a reduced number of devices, showcasing that a 1:2:4:8 source ratio can effectively maximize the number of output levels. This binary approach allows for a significant reduction in THD compared to symmetric configurations, which usually require more switches for the same number of levels [8]. Furthermore, the transition from high-frequency Pulse Width Modulation (PWM) to fundamental-frequency switching has been documented as a superior method for reducing switching losses in high-level inverters [4]. Despite these advancements, the literature highlights a persistent challenge: maintaining a constant DC-link voltage under varying atmospheric conditions. The integration of battery energy storage systems (BESS) and bidirectional converters has been identified as a robust solution to ensure a "stiff" DC link,

thereby providing a stable 31-level staircase waveform even during fluctuations in solar irradiance [3].

III. System Architecture and Proposed Methodology

The proposed methodology is structured to validate the performance of a high-resolution 31-level inverter within a standalone solar-powered framework, specifically tailored for satilities power conversion and to drive industrial-grade induction motor loads. The architecture integrates multiple power electronic stages to ensure that the synthesized energy stability and quality required for real-world heavy-duty applications. The comprehensive system configuration, illustrated in the block diagram below, consists of interconnected subsystems designed for optimal energy harvesting, storage, and conversion.

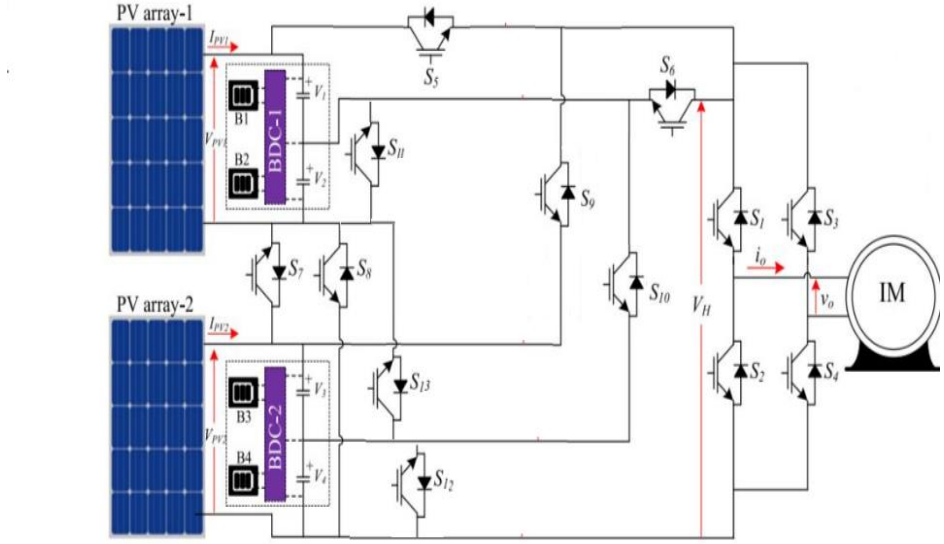

Figure 1. Block Diagram of proposed MLI

The functional stages of the methodology are detailed as follows:

Solar PV Arrays: Utilizing high-efficiency PV arrays, this stage extracts maximum power through the Incremental Conductance (IC) MPPT algorithm. This ensures that the energy input is optimized even under fluctuating atmospheric conditions.

Batteries Storage: To address the intermittency of solar irradiance, a Battery Energy Storage System (BESS) is integrated. Each battery unit is coupled with a bidirectional DC-DC converter, which serves the dual purpose of maintaining a "stiff" DC-link voltage and managing the energy flow during charging and discharging cycles.

Multilevel Inverter: The core of the methodology lies in the 13-switch 31-level inverter. By adopting a binary-weighted source management strategy (1:2:4:8 ratio), the system synthesizes a high-fidelity staircase waveform. This stage is governed by a fundamental-frequency switching logic, which is strategically designed to minimize harmonic distortion and switching losses.

Induction Motor Load: The final stage involves driving a 2.5 kW induction motor. The methodology focuses on evaluating the motor's performance in terms of speed stability and torque ripples, ensuring that the inverter's low THD output (0.11% current THD) translates into efficient mechanical operation without the need for external filtering.

IV. Bidirectional Converter Operation

The bidirectional DC-DC converter (BDC) serves as the critical interface between the energy storage units and the multilevel inverter's DC-link stages. The BDC is tasked with maintaining the equilibrium between stochastic PV generation and dynamic load requirements. Its primary objective is to regulate the DC-link capacitors to their specific binary-weighted potentials, ensuring the integrity of the 31-level output waveform regardless of environmental fluctuations.

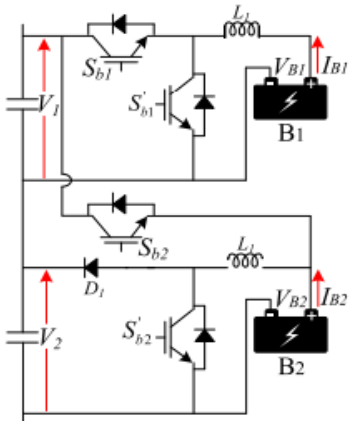

Figure 2. Bidirectional Converter

The converter utilizes a non-isolated half-bridge topology, characterized by a complementary switching pair that allows for two-quadrant operation. The direction of current through the interfacing inductor determines the operational mode, which is governed by the voltage differential between the battery bank and the DC-link capacitor.

- **Buck Operation** (Charging Mode): This mode is initiated during intervals of high solar irradiance where the power generated by the PV arrays exceeds the consumption of the 2.5 kW induction motor. The upper semiconductor switch is pulse-width modulated while the lower switch remains inactive. In this state, the converter steps down the higher DC-link voltage to a level suitable for battery charging. The inductor stores energy during the "ON" period and discharges it into the battery during the "OFF" period through the anti-parallel diode of the lower switch, effectively replenishing the storage reservoir.

- **Boost Operation** (Discharging Mode): During periods of partial shading, cloud transients, or zero-irradiance (nocturnal operation), the system transitions into boost mode. Here, the lower switch is modulated, and the upper switch remains open. The inductor current ramps up, storing energy from the battery; when the switch is turned off, the combined energy of the battery and the inductor is forced through the anti-parallel diode of the upper switch into the DC-link capacitor.

V. Switching Angle Calculation

The optimization of the 31-level staircase waveform relies on the precise determination of switching angles (α1, α2.….α15) within a fundamental cycle. To achieve a near-sinusoidal profile and minimize the Total Harmonic Distortion (THD), the fundamental-frequency switching strategy is employed. The angles are derived by equating the instantaneous output voltage to the reference sine wave at specific sampling intervals. For a 31-level resolution, the transition points are calculated using the transcendental equation:

$$\alpha_i = \sin^{-1}\left(\frac{i - 0.5}{15}\right) \text{ for } i = 1, 2, \ldots, 15$$

This methodology ensures that each of the 15 voltage steps in the positive half-cycle is triggered at the optimal temporal position. By maintaining symmetry across the 90 degrees and 180 degrees axes, even-order harmonics are inherently eliminated. This precise timing allows the system to satisfy stringent power quality criteria without requiring high-frequency modulation, thereby significantly reducing switching-related power dissipation and thermal stress on the semiconductor switches.

VI. MLI OPERATIONAL MODES

The synthesis of the 31-level output voltage is achieved through the coordinated switching of the 13 semiconductor devices. The operational sequence is divided into distinct intervals based on the additive and subtractive combinations of the binary-weighted DC sources (V1 to V4).

A. Operating Modes: Levels 1 to 5

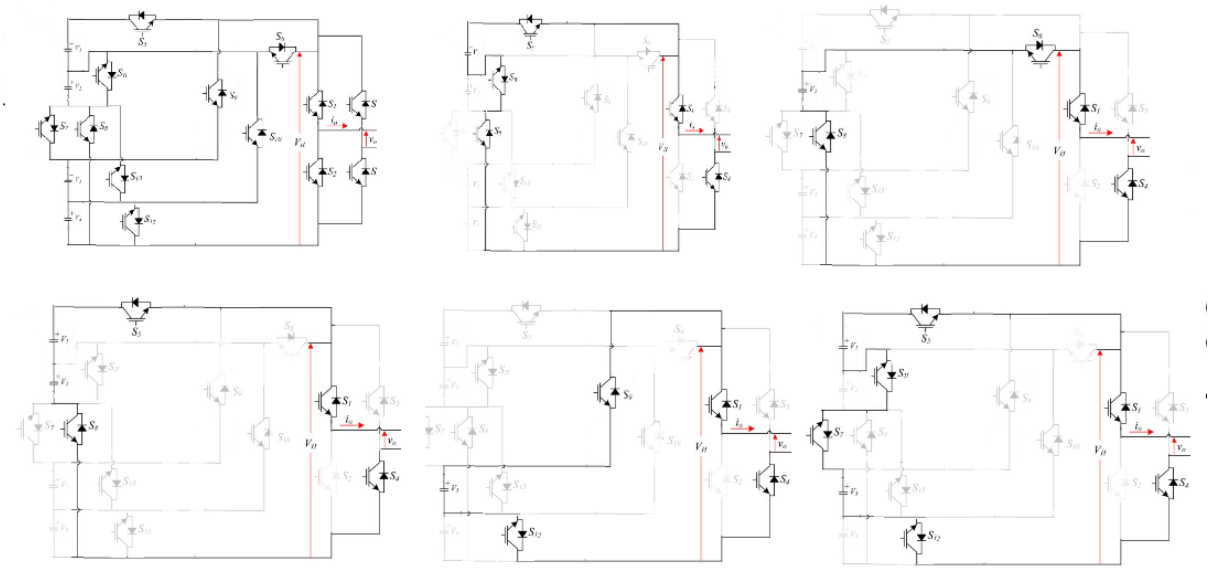

Figure 3. MLI Operating from 1 to 5 Levels

In the initial conduction phase, the inverter synthesizes levels 1 through 5 by utilizing lower-order source combinations. Level 1 is generated by activating V1 (26V) independently. Subsequent levels are formed by the sequential addition of V2 (52V) and its combinations with

V1. These modes involve minimal switch transitions, ensuring a smooth start to the staircase profile while maintaining low dv/dt stress during the nascent stages of the fundamental cycle.

B. Operating Modes: Levels 6 to 11

Figure 4. MLI Operating from 6 to 7 Levels

This intermediate section involves more complex switching states to bridge the voltage gap between mid-range and high-range potentials. Levels 6 through 11 are primarily synthesized by integrating V3 (103V) into the conduction path. The control logic combines V3 with various permutations of V1 and V2 to maintain the 26V step resolution. This phase is critical for maintaining waveform linearity as the output approaches the peak fundamental value, requiring precise synchronization of the intermediate gate pulses.

C. Operating Modes: Levels 12 to 15

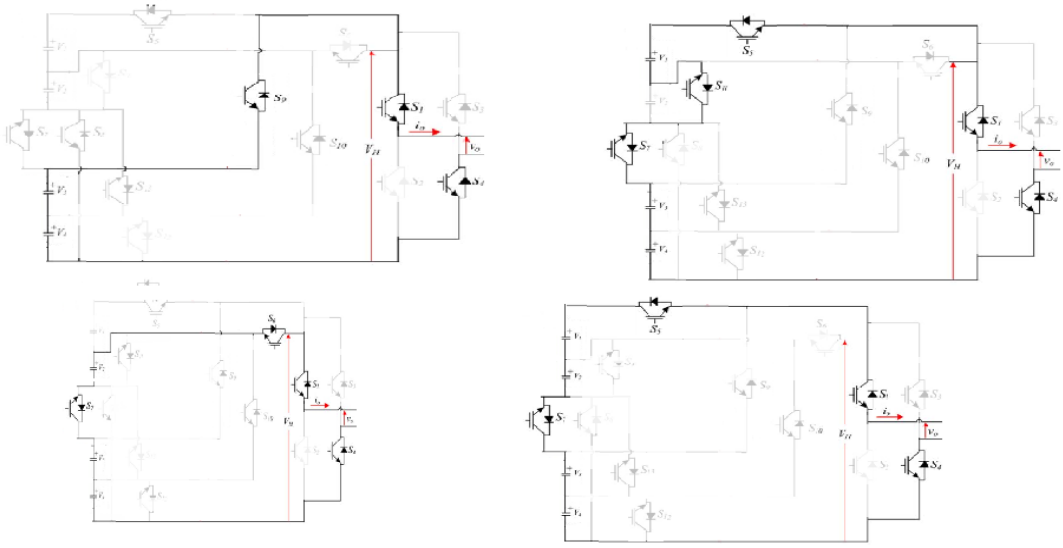

Figure 5. MLI Operating from 12 to 15 Levels

The final operational phase reaches the peak amplitude of the 31-level waveform. Level 12 initiates the inclusion of the highest binary source, V4 (205V), which is then incremented by the remaining sources to reach the maximum peak of 386V at level 15. The switching logic ensures that the cumulative potential of all four sources is utilized at the peak of the sine wave reference. Following this, the sequence is mirrored to initiate the descending staircase, effectively completing the high-resolution power conversion.

VII. DC-LINK AND POWER CONTROL STRATEGY

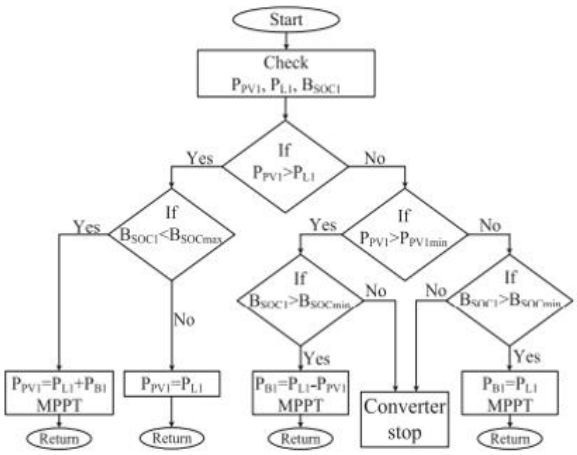

Figure 6. Power flow control strategy

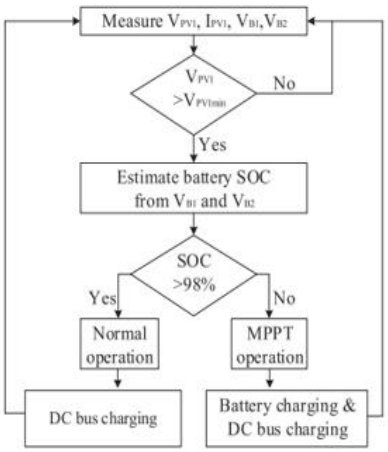

Figure 7. DC link control strategy

The stability of the 31-level output is governed by a dual-stage control framework focused on DC-link regulation and optimal power extraction. To maintain the 1:2:4:8 binary ratio, a closed-loop voltage control strategy is implemented using proportional-integral (PI) regulators. These controllers adjust the duty cycles of the bidirectional DC-DC converters, balancing the potential across each capacitor regardless of solar transients. Simultaneously, the power control strategy utilizes an Incremental Conductance MPPT algorithm to harvest maximum energy from the PV arrays. This coordinated approach ensures that the battery storage effectively compensates for power deficits, providing a constant, ripple-free DC bus. This dual-layer regulation is vital for minimizing torque pulsations in the induction motor and ensuring the current THD remains at a negligible 0.11%.

VIII. SIMULATION MODELING

The simulation of proposed MLI with standalone PV system simulated by MATLAB Simulink. The Simulink model consists of interconnected subsystems, including the PV array, electric motor, MLI, batteries and BDC block. The simulation parameters are defined based on a induction motor with a rated power of 2.5 kW. The simulation results will be in two parts, first part consist of uniform irradiance variation and second part is about unequal irradiance variation. Both results are shown separately in two different conditions.

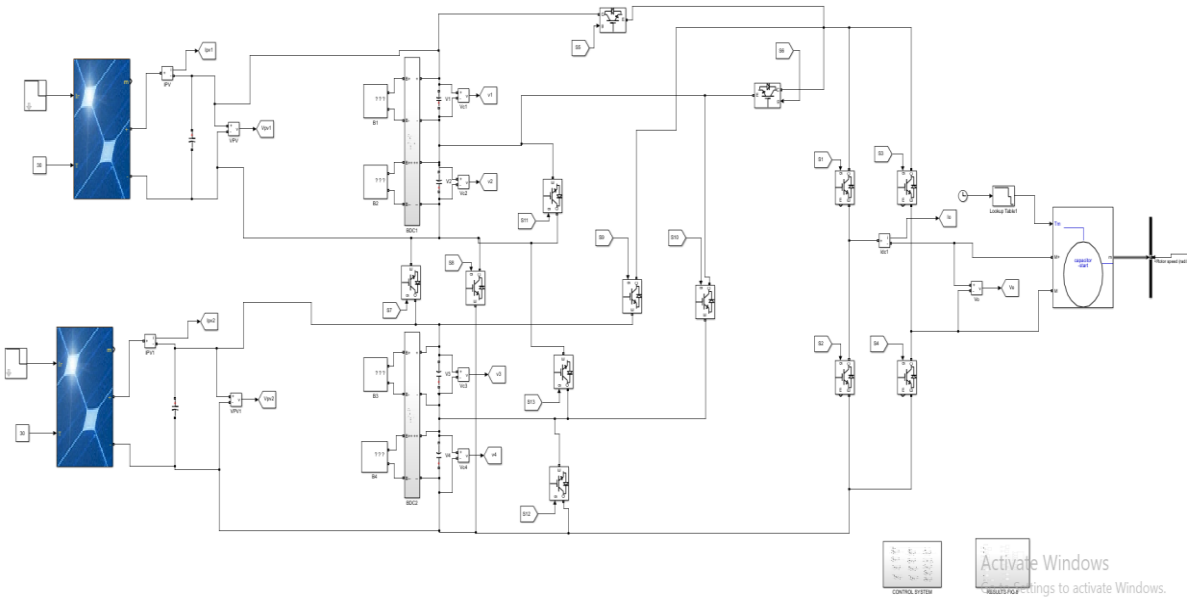

Figure 8. Full Simulation of proposed MLI with PV system

IX. RESULTS AND DISCUSSION

The results are obtained from the two different conditions of PV arrays. They are uniform irradiance variations and unequal irradiance variations.

A. Uniform Irradiance Variations

The performance of the 31-level inverter system under uniform irradiance is evaluated by observing the waveforms of the output voltage (vo), output current (io), PV array parameters, DC-link capacitor voltages (VC1 to VC4), and battery currents (IB1 to IB4). The analysis is divided into three distinct operational phases based on the solar irradiance levels applied to both PV arrays.

Phase 1: Standard Irradiance (0s to 0.5s)

Operating at a standard irradiance of 1000 W/m^2, the PV arrays autonomously full fill the 2.5 kW load requirement. During this interval, the battery units remain in a standby state with zero current (I{B1-B4} = 0), while the state-of-charge (SOC) remains stable. The DC-link capacitors maintain their precise binary-weighted potentials, facilitating a high-resolution 31-level staircase output.

Phase 2: Partial Irradiance Fall (0.5s to 0.8s)

Upon a 50% reduction in irradiance (down to 500 W/m^2), the PV generation decreases proportionally. To mitigate this power deficit, the bidirectional converters instantly initiate the discharging of the battery units. The battery currents transition to positive values, injecting the

necessary power into the DC-link to sustain the 386V peak output without compromising waveform quality.

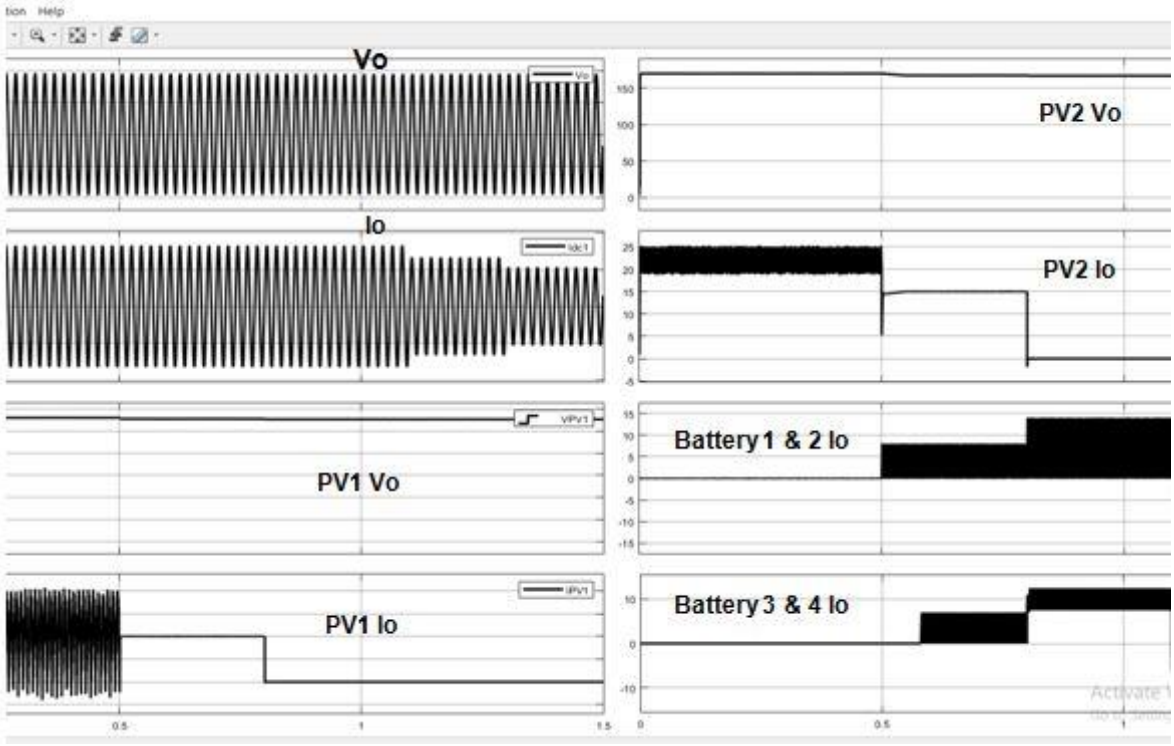

Figure 9. Performance of the system at uniform irradiance variation

Phase 3: Zero Irradiance (post 0.8s)

Under zero irradiance (deep shading conditions), the PV power output nullifies. The battery energy storage system (BESS) becomes the sole energy source, fully powering the induction motor through the 13-switch inverter. The system maintains a constant voltage profile, validating the robustness of the proposed architecture in ensuring uninterrupted, high-quality power delivery for standalone renewable applications.

B. Performance under Unequal Irradiance Conditions

The bidirectional DC-DC converters (BDC) independently regulate DC-link potentials to preserve a high-fidelity 31-level output during source imbalances.

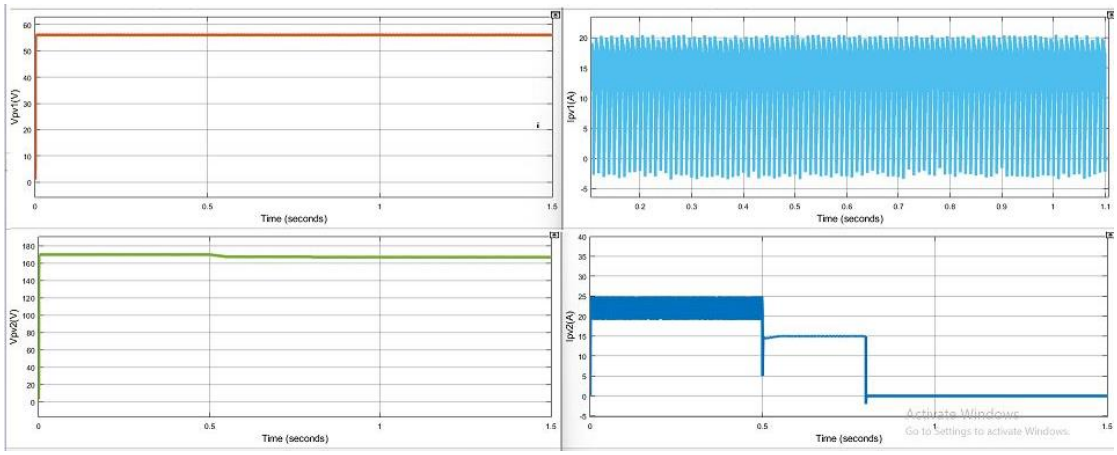

Figure 10. PV arrays voltages and currents at unequal irradiance variation

Initially, at a uniform irradiance of 1000 W/m^2 (0s to 0.4s), both PV arrays satisfy the 2.5 kW load demand symmetrically. At t=0.4s, a mismatch is introduced by reducing the irradiance on PV Array-1 to 500 W/m^2. The control system responds by triggering battery units B1 and B2 into discharge mode through BDC-1 to compensate for the power deficit. At t=0.7s, when PV Array-2 also drops to 500 W/m^2, all battery units (B1–B4) engage simultaneously to maintain the cumulative DC-link potential.

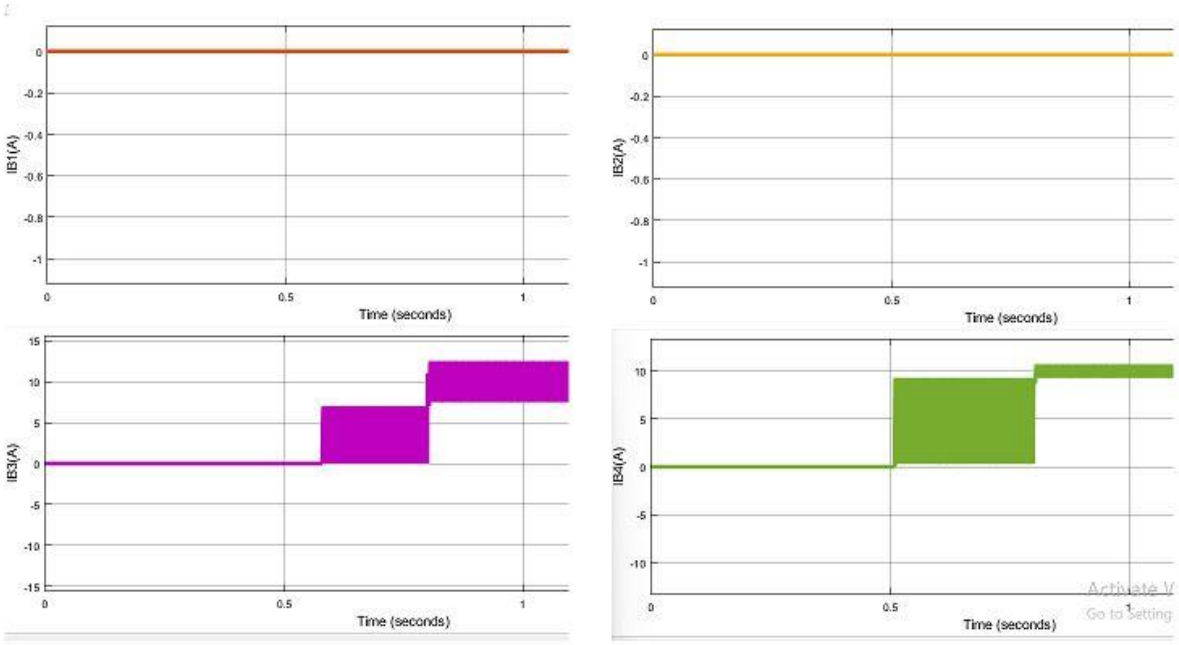

Figure 11. Currents of batteries at unequal irradiance variation

Throughout these transitions, the inverter output voltage maintains its stable 386V peak and 31-level resolution. This demonstrates that the binary-weighted source ratio (1:2:4:8) remains intact due to the robust closed-loop management of the BESS, ensuring consistent power quality despite sudden environmental changes.

X. Output Voltage THD Analysis

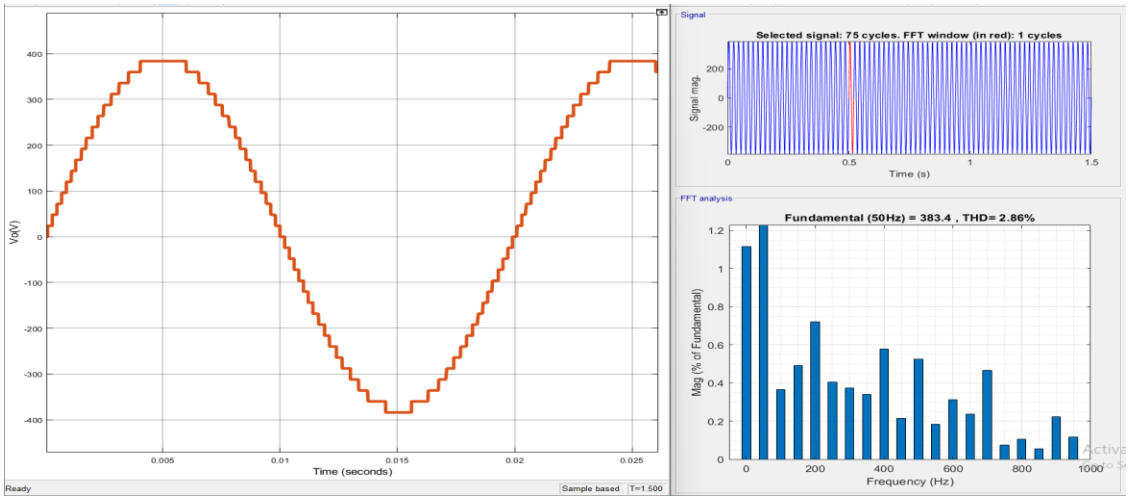

Figure 12. Output voltage THD

The spectral integrity of the 13-switch 31-level inverter is rigorously evaluated through Fast Fourier Transform (FFT) analysis. This assessment is vital to ensure the synthesized energy meets the stringent power quality requirements for industrial-grade induction motor drives.

1. **Waveform Fidelity:** The simulated output voltage (vo) exhibits a high-resolution staircase profile comprising 31 discrete levels (15 positive, 15 negative, and one zero-voltage step). This high-order synthesis produces a waveform that closely approximates a pure sinusoidal reference, inherently suppressing the magnitude of lower-order harmonics at the source.
2. **THD Compliance:** The spectral analysis confirms a Total Harmonic Distortion (THD) of 2.86% for the output voltage. This result is significantly lower than the 5% threshold mandated by the IEEE standards, validating the inverter's suitability for sensitive motor-driven applications without auxiliary filtering.
3. **Spectral Distribution:** The harmonic spectrum demonstrates that the fundamental 50Hz component retains dominant power, while higher-order harmonics are maintained at negligible levels. The implementation of optimized switching angles ensures the effective mitigation of the 5th, 7th, and 11th harmonic orders, thereby reducing torque pulsations and thermal losses within the induction motor load.

XI. Output Current THD Analysis

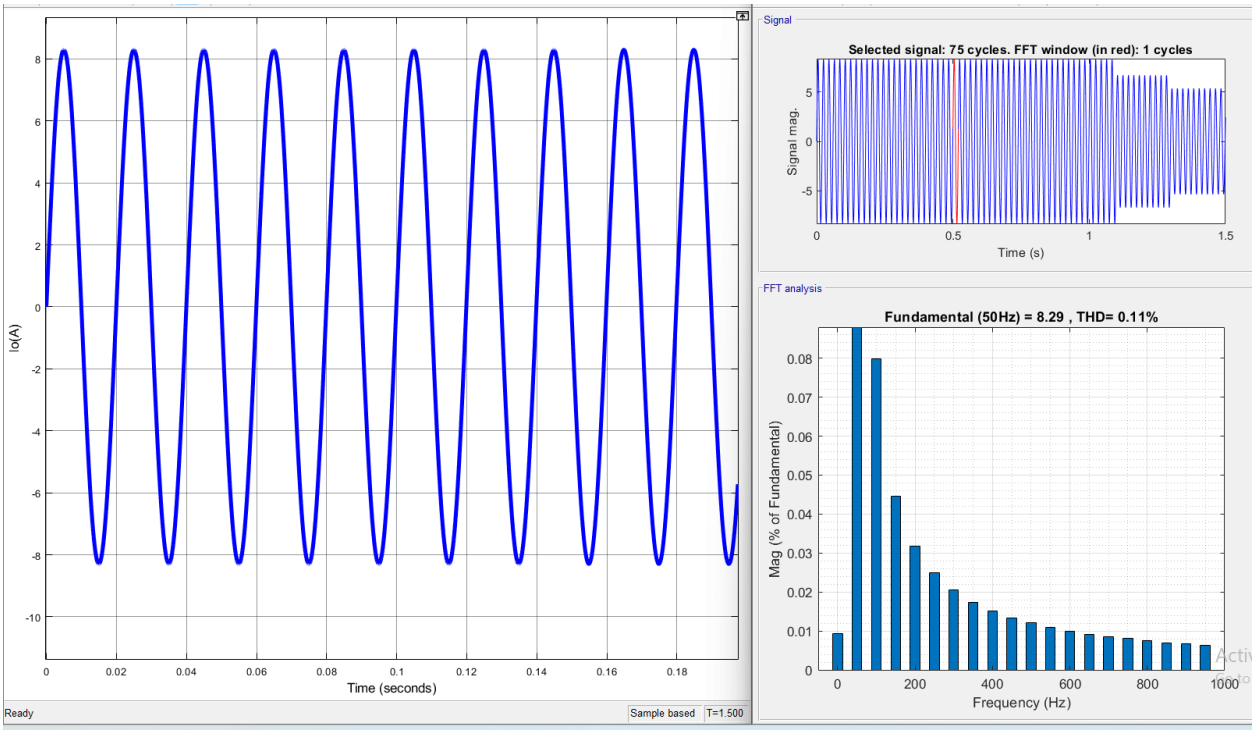

Figure 13. Output current THD

Above figure shows the harmonic analysis of the output current (io) is examined to evaluate the quality of power delivered to the 2.5 kW induction motor. Due to the inherent inductive nature of the motor windings, the load acts as a natural low-pass filter, which further smoothen the 31-level staircase current wave form. The FFT analysis reveals an exceptionally low Total Harmonic Distortion for the output current, measured at **0.11%**. This value represents a superior level of power quality, ensuring that the motor operates with negligible harmonic interference. The motor's internal inductance effectively suppresses the high-frequency

switching components, ensuring that the current harmonics do not contribute to torque pulsations or vibration.

XII. Conclusion

The proposed research successfully validates a 13-switch 31-level inverter integrated with a PV-battery hybrid system, specifically engineered to drive a 2.5 kW induction motor with high efficiency and superior power quality. By adopting a binary-weighted DC source configuration (1:2:4:8 ratio), the architecture achieves high-resolution voltage steps with a minimized semiconductor count, effectively reducing system cost and complexity. Simulation results across diverse conditions, including unequal irradiance variations, demonstrate that the coordinated control of bidirectional DC-DC converters maintains stable DC-link potentials and a consistent 386V peak output. The system's primary strength is its exceptional harmonic performance, yielding a voltage THD of 2.86% and a current THD of 0.11%, which significantly exceed IEEE 519-2014 standards and eliminate the necessity for bulky external filters. Furthermore, the 26V step increments mitigate dv/dt stress on motor windings, while the integrated battery storage ensures reliable, continuous operation during zero-irradiance periods, establishing this topology as a robust solution for standalone industrial renewable energy applications.

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